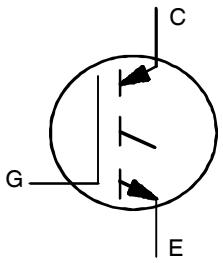
International
IOR Rectifier

IRG7PH50UPbF
IRG7PH50U-EP

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Low $V_{CE\ (ON)}$ trench IGBT technology
- Low switching losses
- Maximum junction temperature 175 °C
- Square RBSOA
- 100% of the parts tested for I_{LM}
- Positive $V_{CE\ (ON)}$ temperature co-efficient
- Tight parameter distribution
- Lead-Free



n-channel

V_{CES} = 1200V

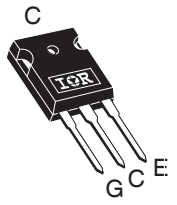
I_C = 90A, T_C = 100°C

$T_{J(max)}$ =175°C

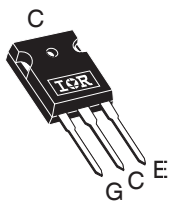
$V_{CE(on)}$ typ. = 1.7V

Benefits

- High efficiency in a wide range of applications
- Suitable for a wide range of switching frequencies due to low $V_{CE\ (ON)}$ and low switching losses
- Rugged transient performance for increased reliability
- Excellent current sharing in parallel operation



TO-247AC
IRG7PH50UPbF



TO-247AD
IRG7PH50U-EP

Applications

- U.P.S
- Welding
- Solar inverter
- Induction heating

G	C	E
Gate	Collector	Emitter

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current (Silicon Limited)	140	A
I_C @ T_C = 100°C	Continuous Collector Current (Silicon Limited)	90	
$I_{NOMINAL}$	Nominal Current	50	
I_{CM}	Pulse Collector Current, V_{GE} = 15V	150	
I_{LM}	Clamped Inductive Load Current, V_{GE} = 20V ①	200	
V_{GE}	Continuous Gate-to-Emitter Voltage	±30	V
P_D @ T_C = 25°C	Maximum Power Dissipation	556	W
P_D @ T_C = 100°C	Maximum Power Dissipation	278	
T_J	Operating Junction and	-55 to +175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT) TO-247AC ④	—	—	0.27	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface) ④	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	40	—	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 100µA ③
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.0	—	V/°C	V_{GE} = 0V, I_C = 1mA (25°C-150°C) ③
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.7	2.0	V	I_C = 50A, V_{GE} = 15V, T_J = 25°C ②
		—	2.0	—		I_C = 50A, V_{GE} = 15V, T_J = 150°C ②
		—	2.1	—		I_C = 50A, V_{GE} = 15V, T_J = 175°C ②
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	V_{CE} = V_{GE}, I_C = 2.0mA
$\Delta V_{GE(th)}/\Delta TJ$	Threshold Voltage temp. coefficient	—	-17	—	mV/°C	V_{CE} = V_{GE}, I_C = 1mA (25°C - 175°C)
gfe	Forward Transconductance	—	55	—	S	V_{CE} = 50V, I_C = 50A, PW = 80µs
I_{CES}	Collector-to-Emitter Leakage Current	—	2.0	100	µA	V_{GE} = 0V, V_{CE} = 1200V
		—	1700	—		V_{GE} = 0V, V_{CE} = 1200V, T_J = 175°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±200	nA	V_{GE} = ±30V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	290	440	nC	I_C = 50A ②
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	40	60		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	110	170		V_{CC} = 600V
E_{on}	Turn-On Switching Loss	—	3600	4600	µJ	I_C = 50A, V_{CC} = 600V, V_{GE} = 15V ②
E_{off}	Turn-Off Switching Loss	—	2200	3200		R_G = 5.0Ω, L = 200µH,T_J = 25°C
E_{total}	Total Switching Loss	—	5800	7800		Energy losses include tail & diode reverse recovery
$t_{d(on)}$	Turn-On delay time	—	35	55	ns	Diode clamp the same as IRG7PH50UDPbF
t_r	Rise time	—	40	60		
$t_{d(off)}$	Turn-Off delay time	—	430	500		
t_f	Fall time	—	45	65		
E_{on}	Turn-On Switching Loss	—	5600	—	µJ	I_C = 50A, V_{CC} = 600V, V_{GE}=15V ②
E_{off}	Turn-Off Switching Loss	—	3900	—		R_G=5.0Ω, L=200µH, T_J = 175°C
E_{total}	Total Switching Loss	—	9500	—		Energy losses include tail & diode reverse recovery
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	Diode clamp the same as IRG7PH50UDPbF
t_r	Rise time	—	45	—		
$t_{d(off)}$	Turn-Off delay time	—	500	—		
t_f	Fall time	—	210	—		
C_{ies}	Input Capacitance	—	6000	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	190	—		V_{CC} = 30V
C_{res}	Reverse Transfer Capacitance	—	130	—		f = 1.0Mhz
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				I_C = 200A V_{CC} = 960V, Vp =1200V Rg = 5.0Ω, V_{GE} = +20V to 0V, T_J =175°C

Notes:

① V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 200µH, R_G = 5.0Ω.

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.

④ R_θ is measured at T_J of approximately 90°C.

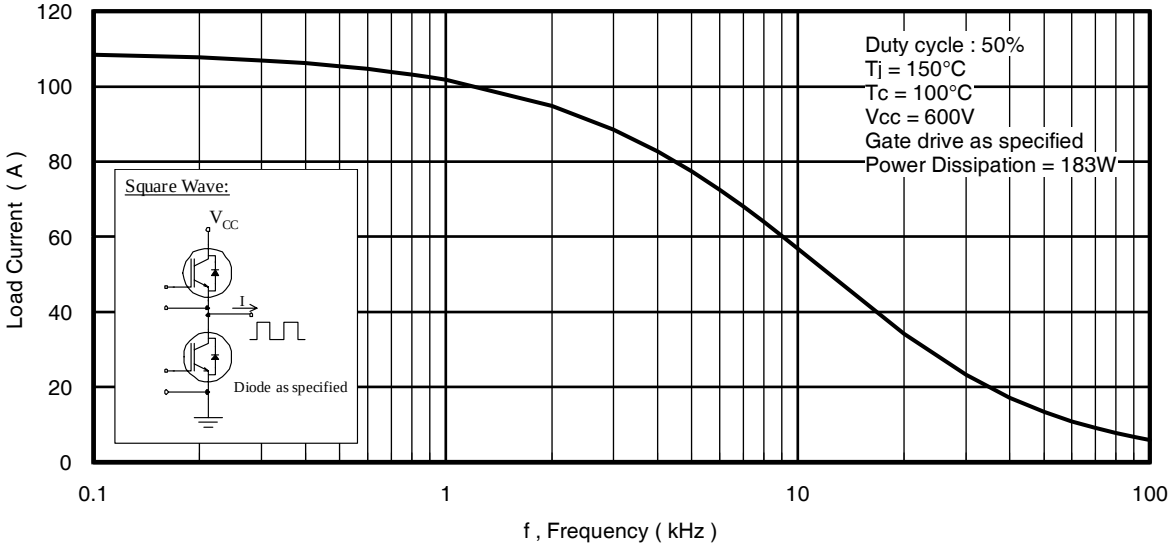


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

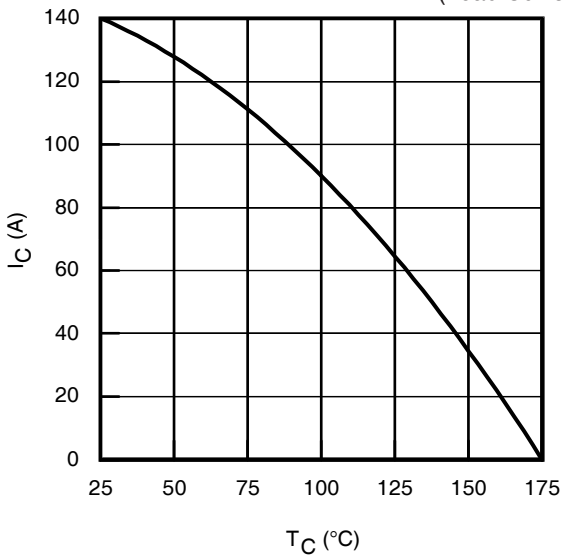


Fig. 2 - Maximum DC Collector Current vs. Case Temperature

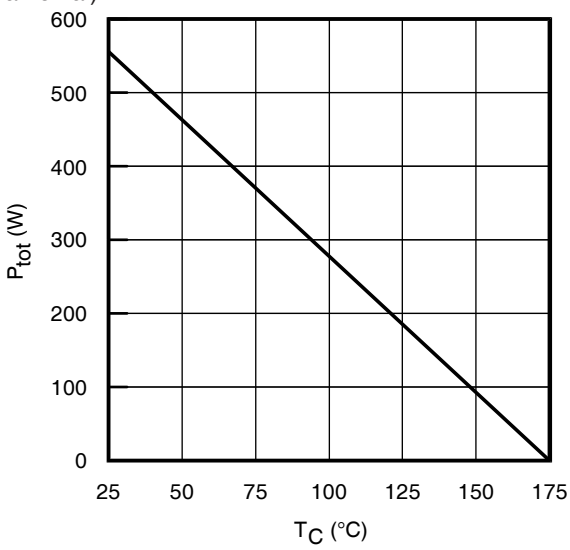


Fig. 3 - Power Dissipation vs. Case Temperature

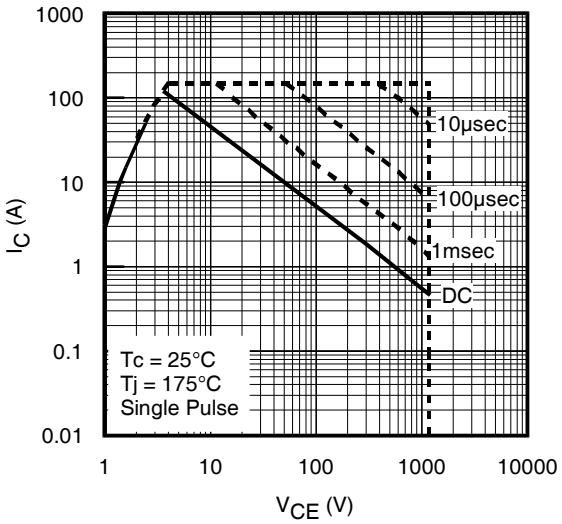


Fig. 4 - Forward SOA
T_C = 25°C, $T_J \leq$ 175°C; V_{GE} =15V

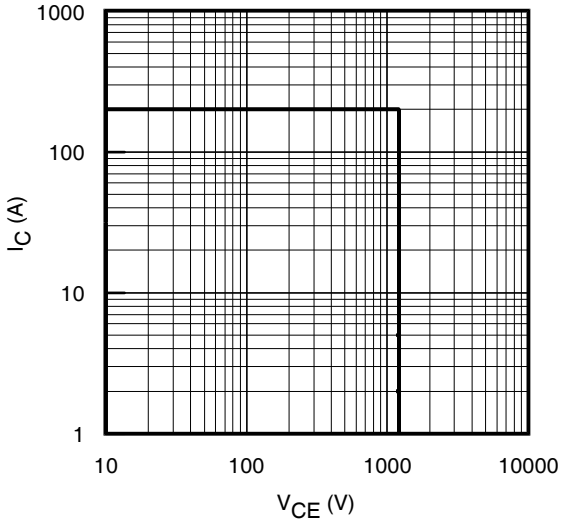


Fig. 5 - Reverse Bias SOA
T_J = 175°C; V_{GE} =20V

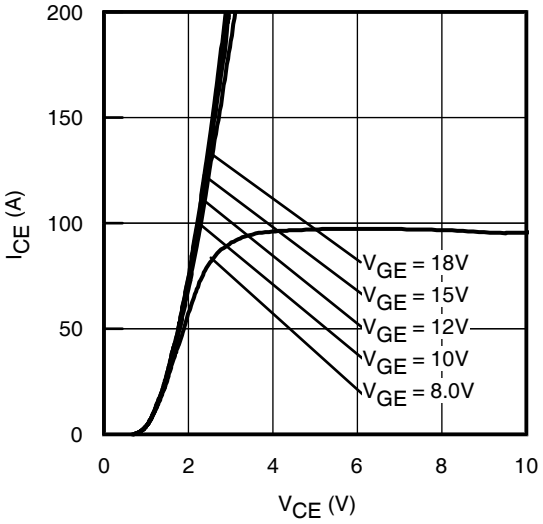


Fig. 6 - Typ. IGBT Output Characteristics
T_J = -40°C; tp = 30µs

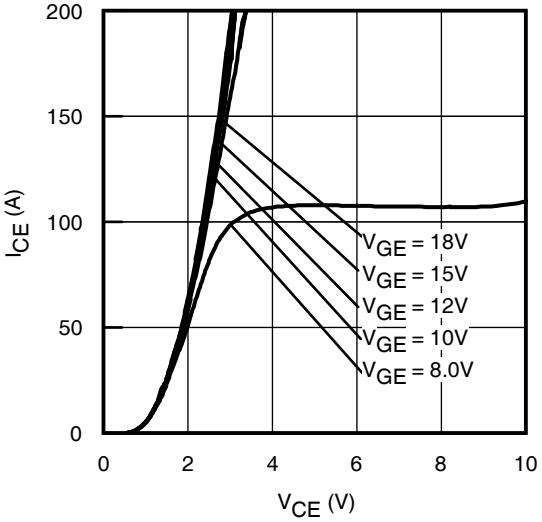


Fig. 7 - Typ. IGBT Output Characteristics
T_J = 25°C; tp = 30µs

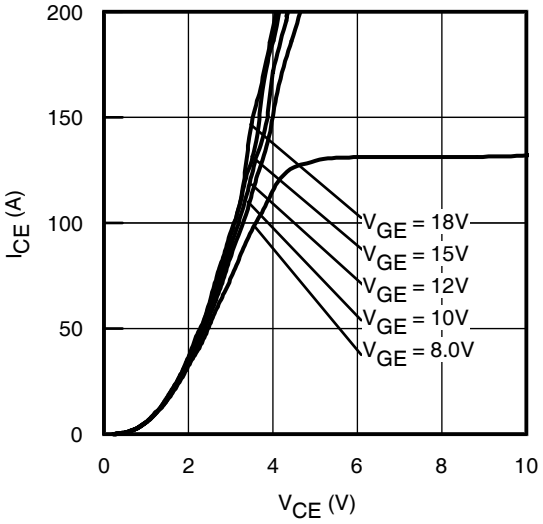


Fig. 8 - Typ. IGBT Output Characteristics
T_J = 175°C; tp = 30µs

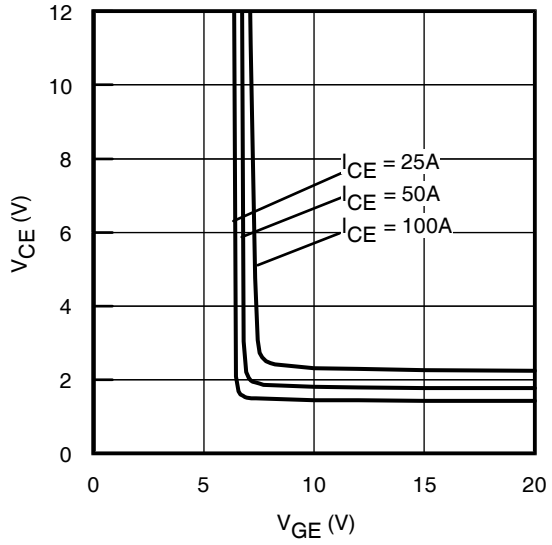


Fig. 9 - Typical V_{CE} vs. V_{GE}
T_J = -40°C

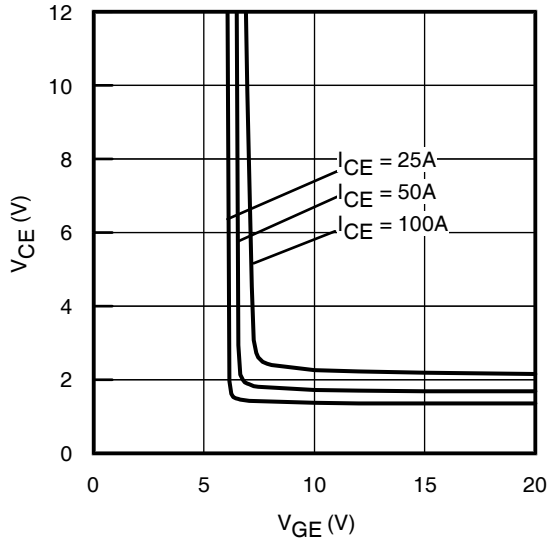


Fig. 10 - Typical V_{CE} vs. V_{GE}
T_J = 25°C

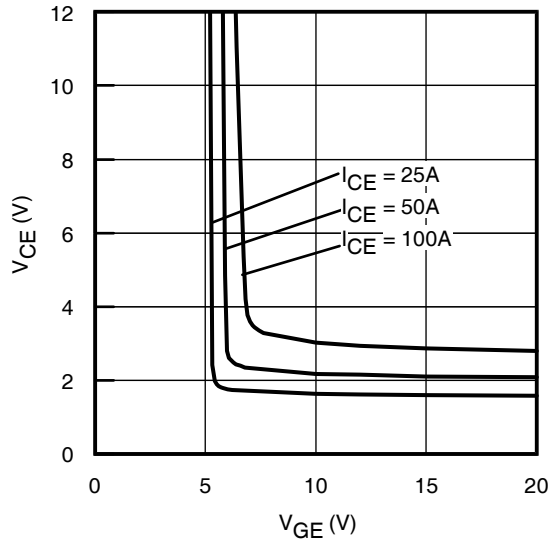


Fig. 11 - Typical V_{CE} vs. V_{GE}
T_J = 175°C

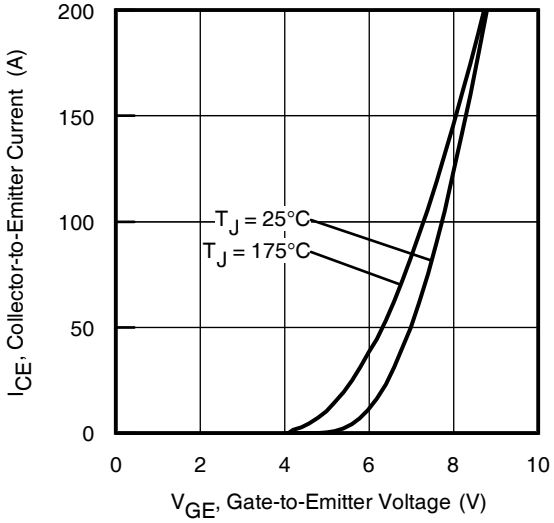


Fig. 12- Typ. Transfer Characteristics
V_{CE} = 50V; tp = 30µs

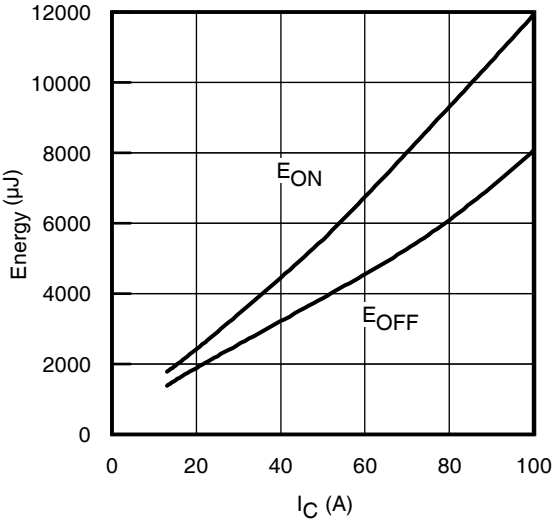


Fig. 13 - Typ. Energy Loss vs. I_C
T_J = 175°C; L = 200µH; V_{CE} = 600V, R_G = 5.0Ω; V_{GE} = 15V

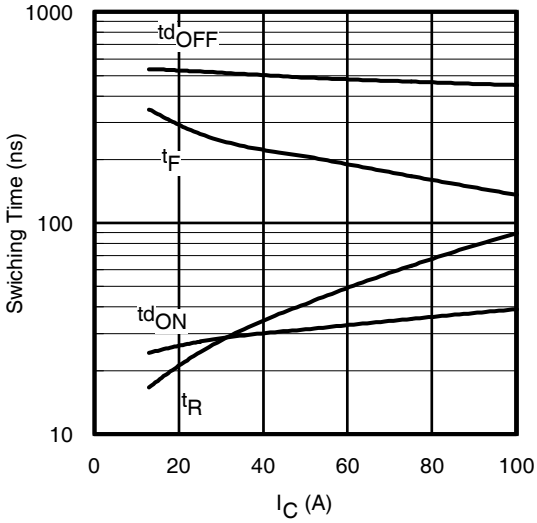


Fig. 14 - Typ. Switching Time vs. I_C
T_J = 175°C; L = 200µH; V_{CE} = 600V, R_G = 5.0Ω; V_{GE} = 15V

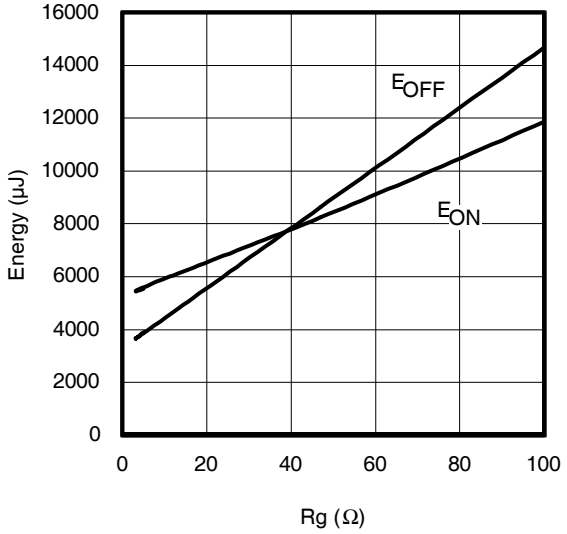


Fig. 15 - Typ. Energy Loss vs. R_G
T_J = 175°C; L = 200µH; V_{CE} = 600V, I_{CE} = 50A; V_{GE} = 15V

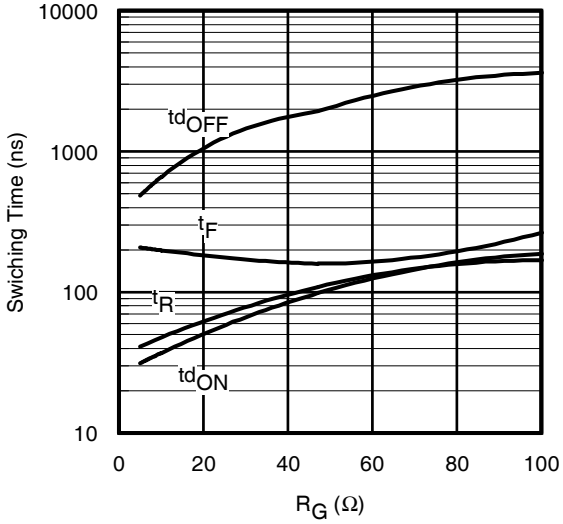


Fig. 16 - Typ. Switching Time vs. R_G
T_J = 175°C; L = 200µH; V_{CE} = 600V, I_{CE} = 50A; V_{GE} = 15V

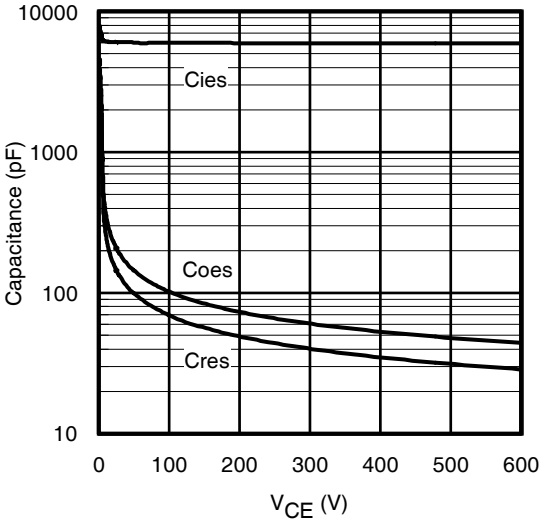


Fig. 17 - Typ. Capacitance vs. V_{CE}
V_{GE}= 0V; f = 1MHz

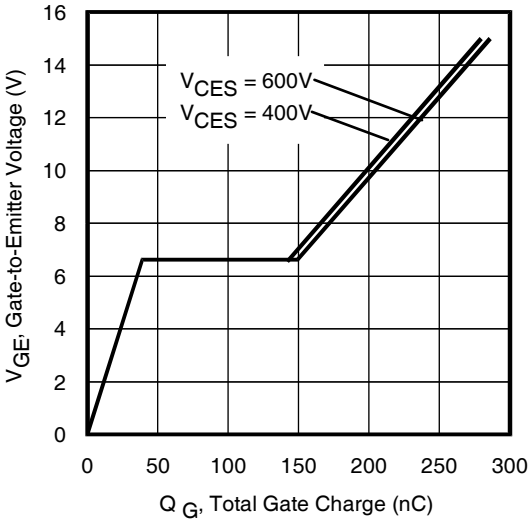


Fig. 18- Typical Gate Charge vs. V_{GE}
I_{CE} = 50A

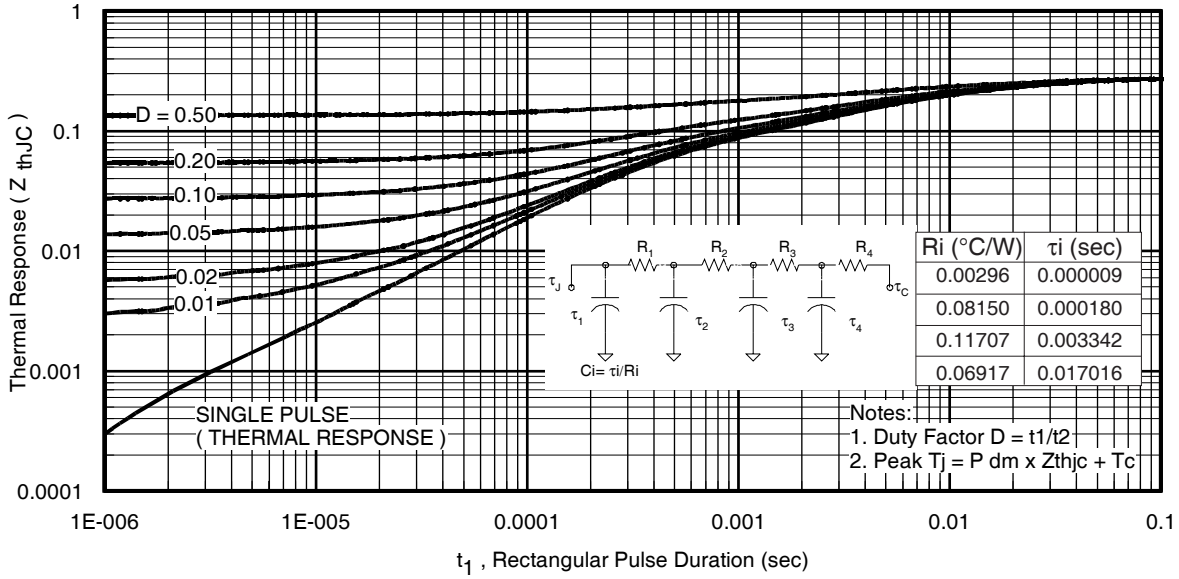


Fig 19. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT) TO-247AC

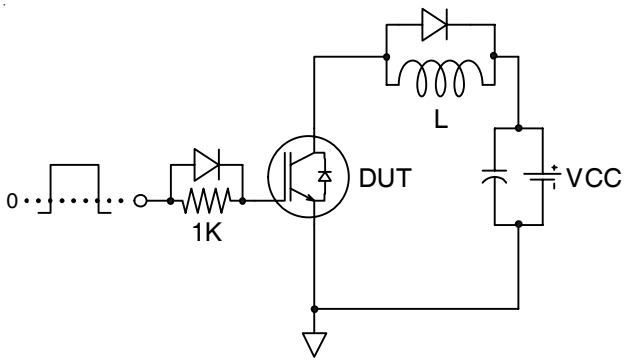


Fig.C.T.1 - Gate Charge Circuit (turn-off)

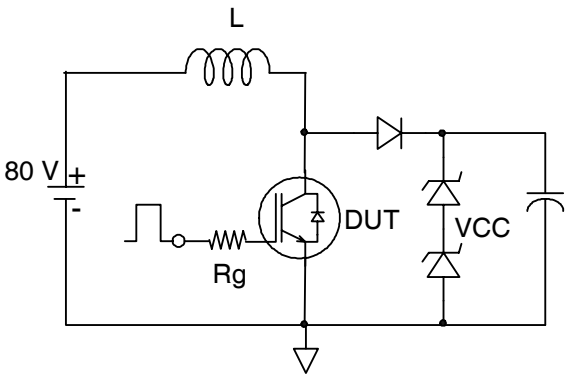


Fig.C.T.2 - RBSOA Circuit

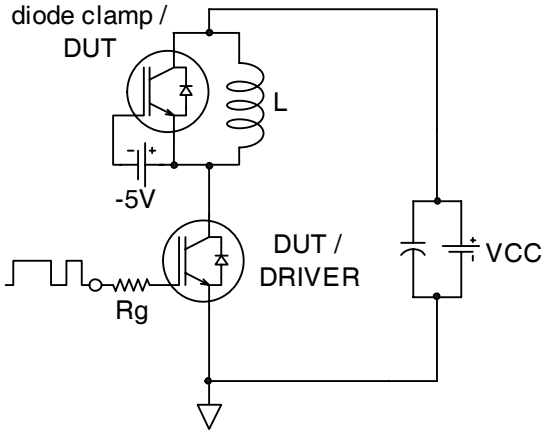


Fig.C.T.3 - Switching Loss Circuit

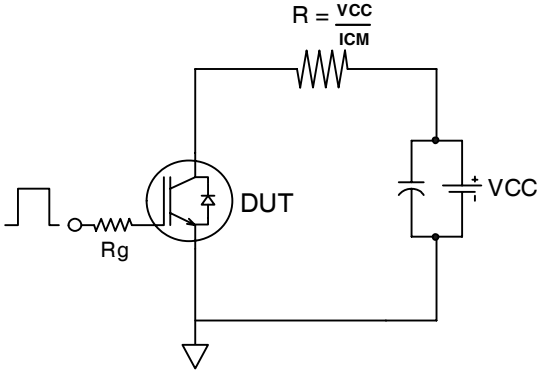


Fig.C.T.4 - Resistive Load Circuit

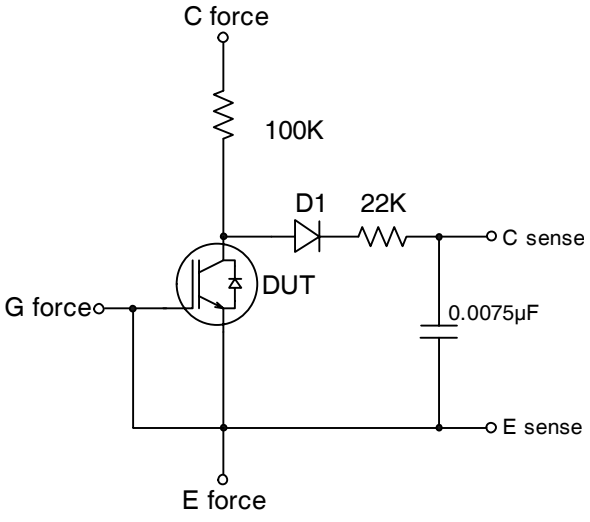


Fig.C.T.5 - BVCES Filter Circuit

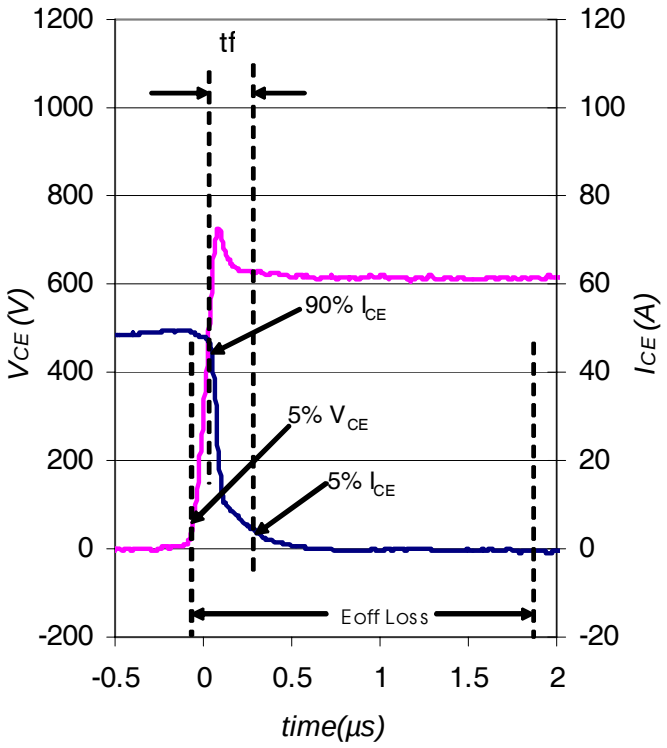


Fig. WF1 - Typ. Turn-off Loss Waveform
@ T_J = 175°C using Fig. CT.4

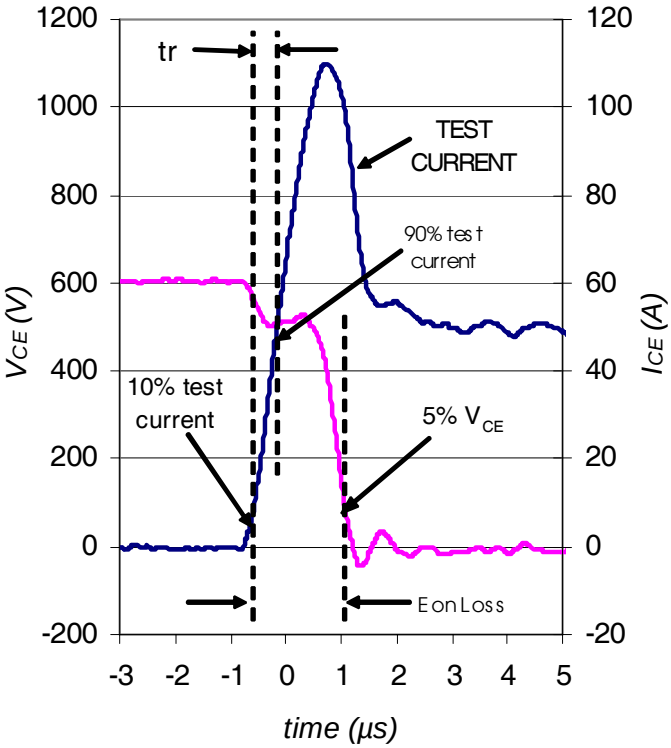
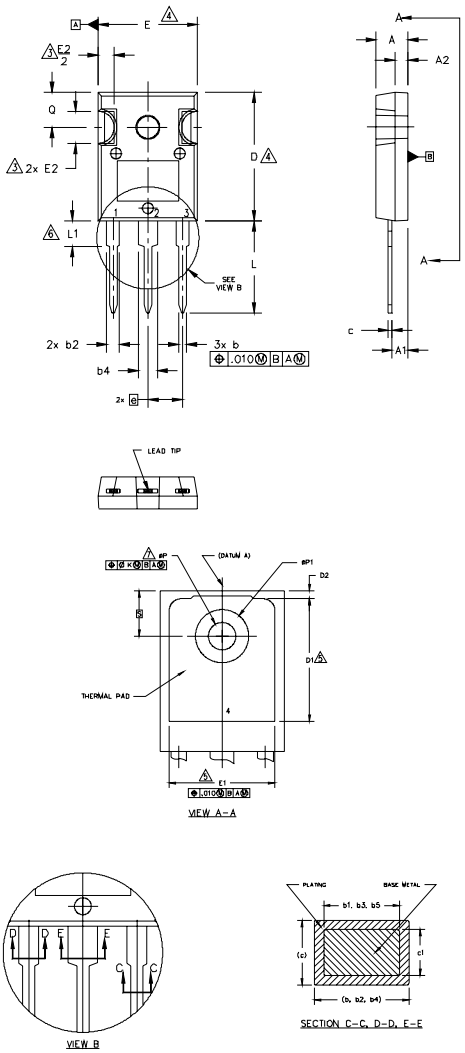


Fig. WF2 - Typ. Turn-on Loss Waveform
@ T_J = 175°C using Fig. CT.4

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

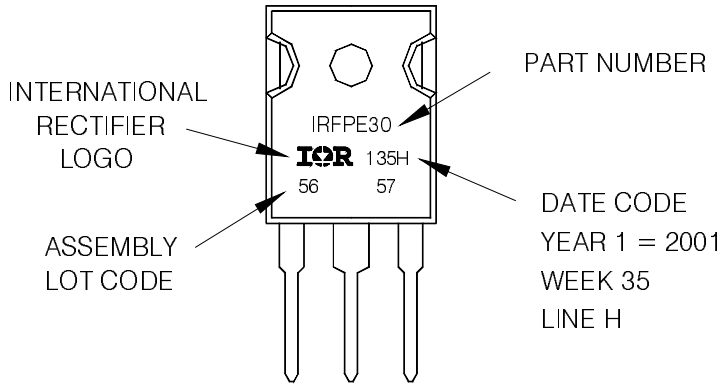
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"

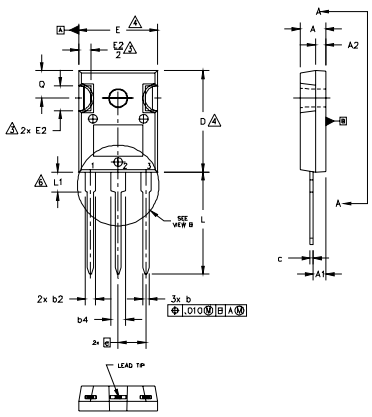


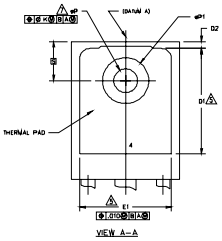
TO-247AC package is not recommended for Surface Mount Application.

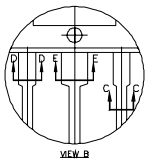
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

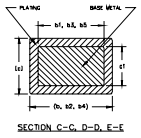
TO-247AD Package Outline

Dimensions are shown in millimeters (inches)









NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

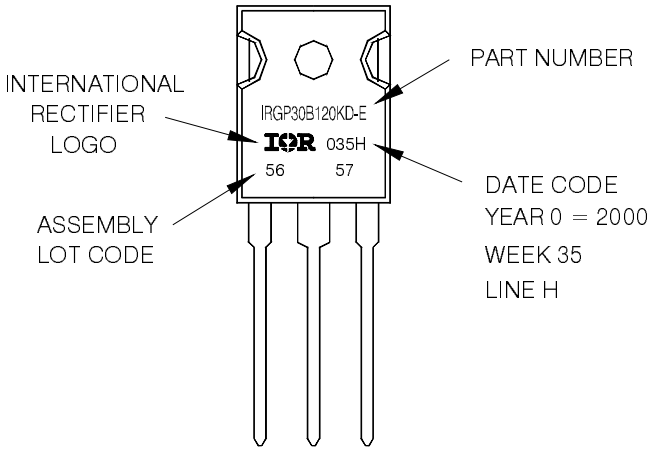
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.

International
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