

# FDWS9510L-F085

## P-Channel Logic Level POWER trench<sup>®</sup> MOSFET

-40 V, -50 A, 13.5 mΩ

### Features

- Typ  $R_{DS(on)}$  = 11 mΩ at  $V_{GS} = -10$  V;  $I_D = -50$  A
- Typ  $Q_{g(tot)}$  = 28 nC at  $V_{GS} = -10$  V;  $I_D = -50$  A
- UIS Capability
- Wettable Flanks for Automatic Optical Inspection (AOI)
- AEC-Q101 Qualified
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-40	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 16$	V
Continuous Drain Current ( $V_{GS} = 10$ V) (Note 1)	$I_D$	-50	A
Pulsed Drain Current		See Figure 4	
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	32	mJ
Power Dissipation	$P_D$	75	W
Derate above $25^\circ\text{C}$		0.5	
Operating and Storage Temperature	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Thermal Resistance (Junction-to-Case)	$R_{\theta JC}$	2	$^\circ\text{C/W}$
Maximum Thermal Resistance (Junction-to-Ambient) (Note 3)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

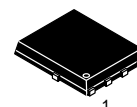
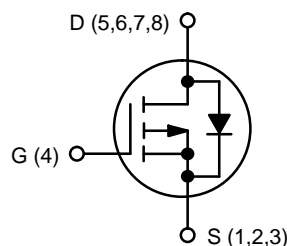
1. Current is limited by wirebond configuration
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 40 \mu\text{H}$ ,  $I_{AS} = -40$  A,  $V_{DD} = -40$  V during inductor charging and  $V_{DD} = 0$  V during time in avalanche
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2 oz copper.



ON Semiconductor<sup>®</sup>

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$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
-40 V	13.5 mΩ @ -10 V	-50 A



DFN8  
Power 56  
CASE 506DW

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

# FDWS9510L-F085

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDWS9510L-F085	FDWS9510L	Power 56	13"	12 mm	3000 units

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

B <sub>VDSS</sub>	Drain-to-Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-40	-	-	V	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C	-	-	1	μA
			T <sub>J</sub> = 175°C (Note 4)	-	-	1	mA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>GS</sub> = ±16 V	-	-	±100	nA	

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250 μA	-1	-1.8	-3	V	
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	I <sub>D</sub> = -25 A, V <sub>GS</sub> = -4.5 V	-	18	23	mΩ	
		I <sub>D</sub> = -50 A V <sub>GS</sub> = -10 V	T <sub>J</sub> = 25°C	-	11	13.5	mΩ
			T <sub>J</sub> = 175°C (Note 4)	-	18.8	23	mΩ

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2320	-	pF
C <sub>oss</sub>	Output Capacitance		-	811	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	38	-	
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> = 0.5 V, f = 1 MHz	-	23	-	Ω
Q <sub>g(tot)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to -10 V	-	28	37	nC
Q <sub>g(th)</sub>	Threshold Gate Charge		V <sub>GS</sub> = 0 to -1 V	-	4	
Q <sub>gs</sub>	Gate-to-Source Gate Charge	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -50 A	-	7	-	
Q <sub>gd</sub>	Gate-to-Drain "Miller" Charge		-	4	-	

### SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	V <sub>DD</sub> = -20 V, I <sub>D</sub> = -50 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω	-	-	20	ns
t <sub>d(on)</sub>	Turn-On Delay Time		-	10	-	
t <sub>r</sub>	Turn-On Rise Time		-	4	-	
t <sub>d(off)</sub>	Turn-Off Delay Time		-	110	-	
t <sub>f</sub>	Turn-Off Fall Time		-	37	-	
t <sub>off</sub>	Turn-Off Time		-	-	222	

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source-to-Drain Diode Voltage	I <sub>SD</sub> = -50 A, V <sub>GS</sub> = 0 V	-	-1	-1.25	V
		I <sub>SD</sub> = -25 A, V <sub>GS</sub> = 0 V	-	-0.9	-1.2	
T <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = -50 A, dI <sub>SD</sub> /dt = 100 A/μs	-	44	62	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	31	47	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T<sub>J</sub> = 175°C. Product is not tested to this condition in production

TYPICAL CHARACTERISTICS

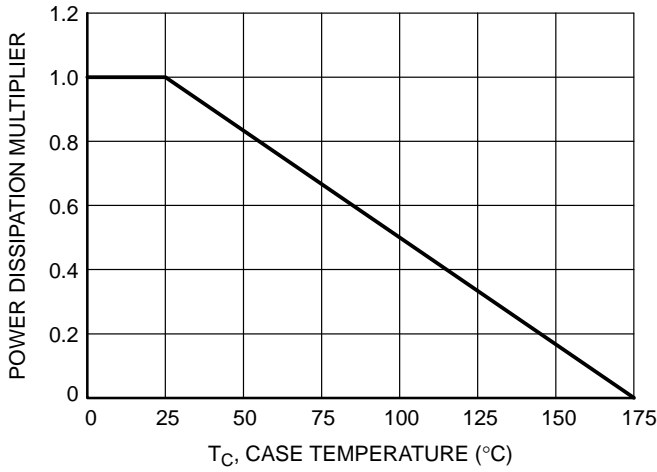


Figure 1. Normalized Power Dissipation vs. Case Temperature

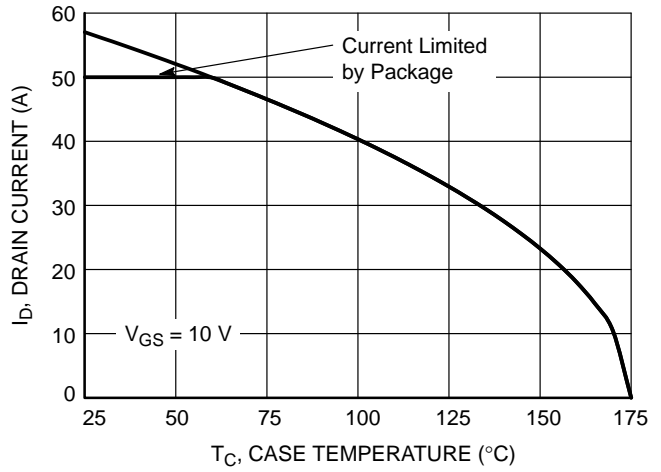


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

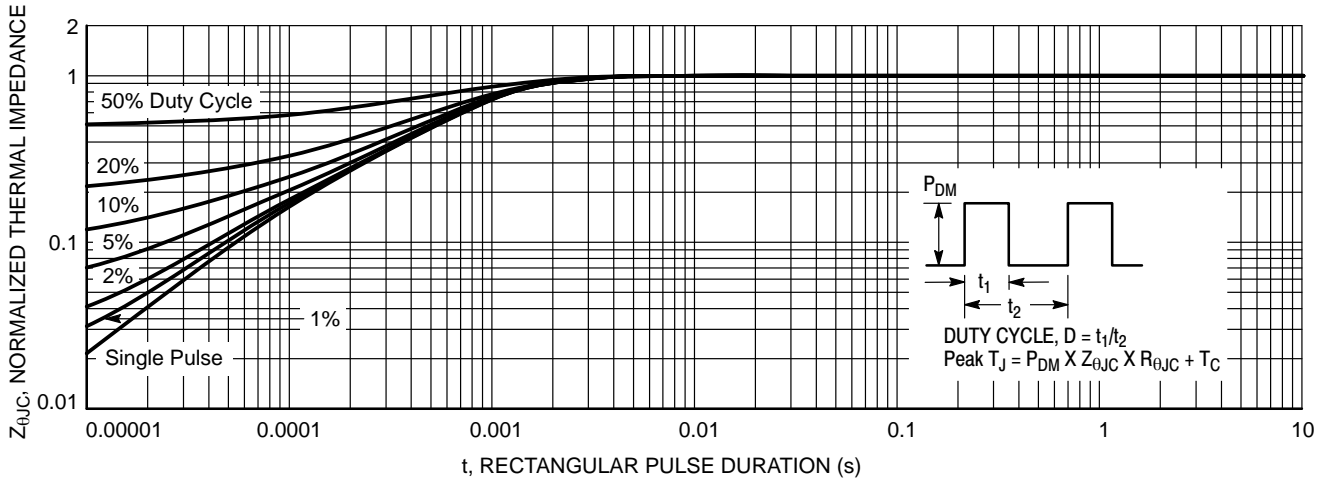


Figure 3. Normalized Maximum Transient Thermal Impedance

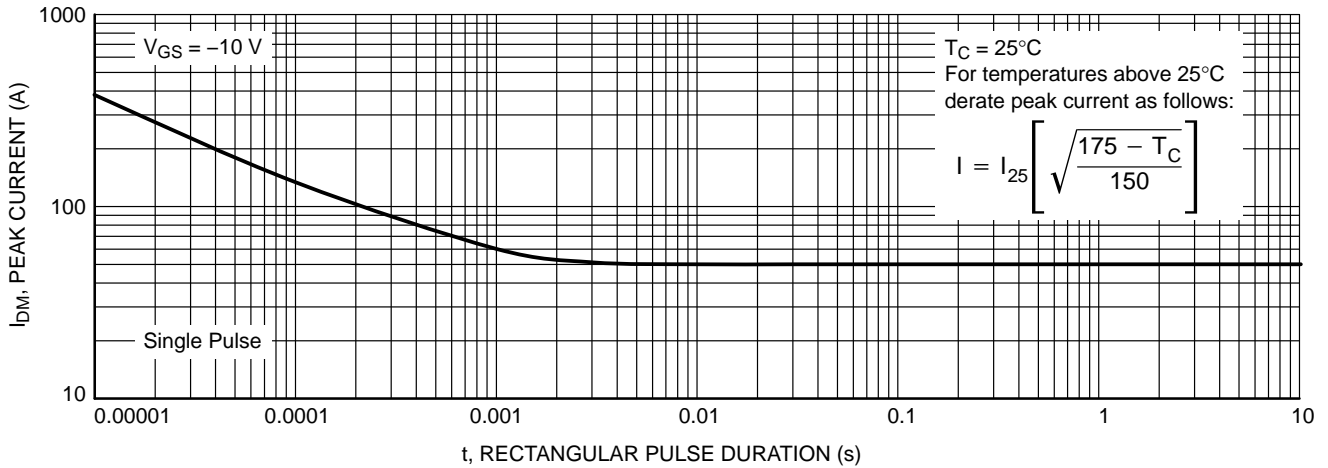


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

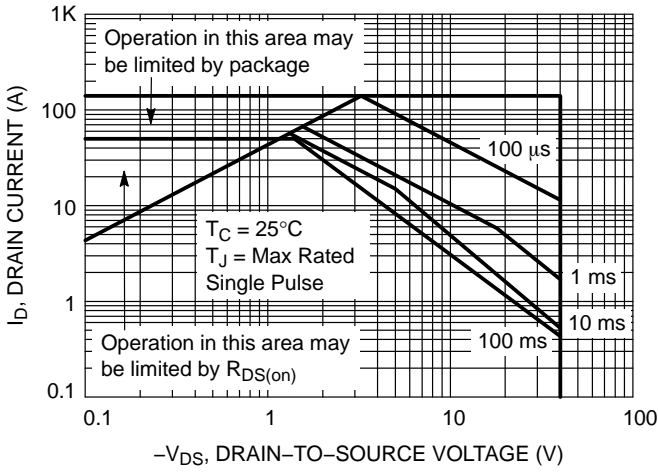


Figure 5. Forward Bias Safe Operating Area

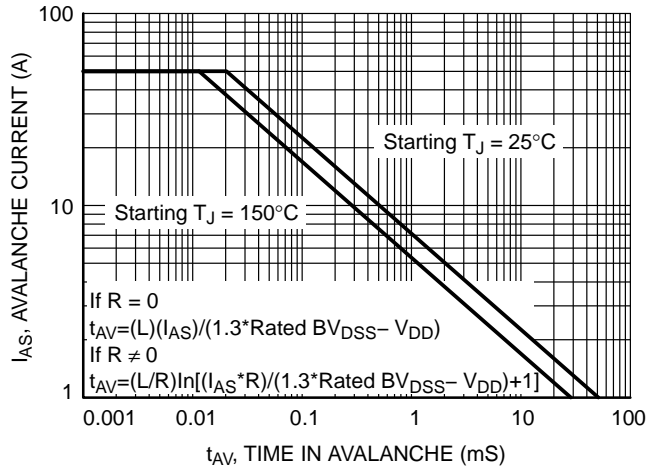


Figure 6. Unclamped Inductive Switching Capability

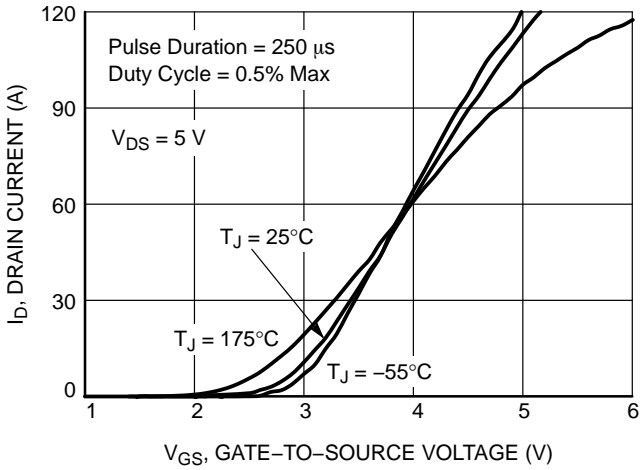


Figure 7. Transfer Characteristics

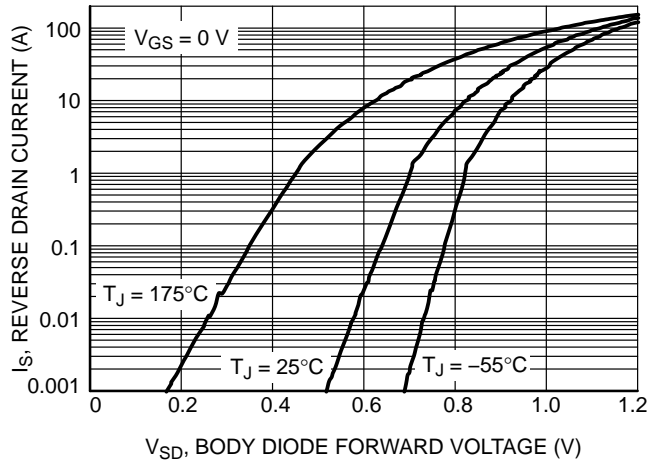


Figure 8. Forward Diode Characteristics

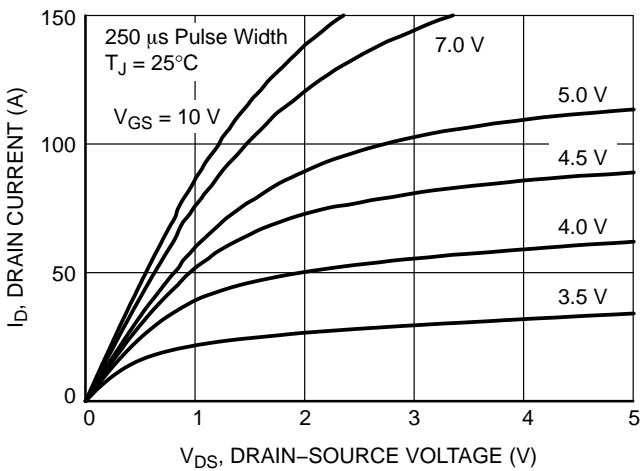


Figure 9. Saturation Characteristics

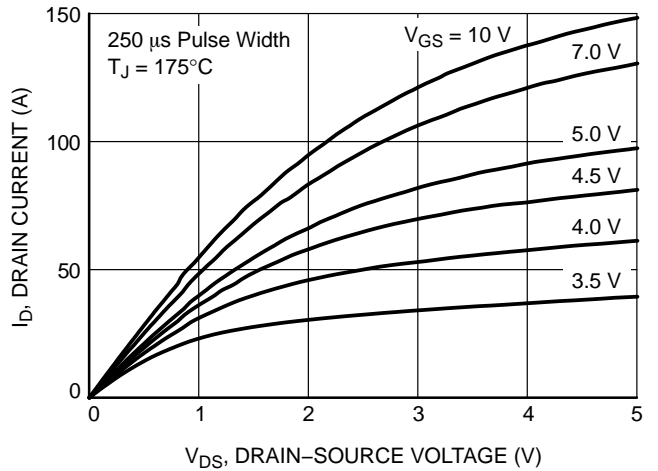


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

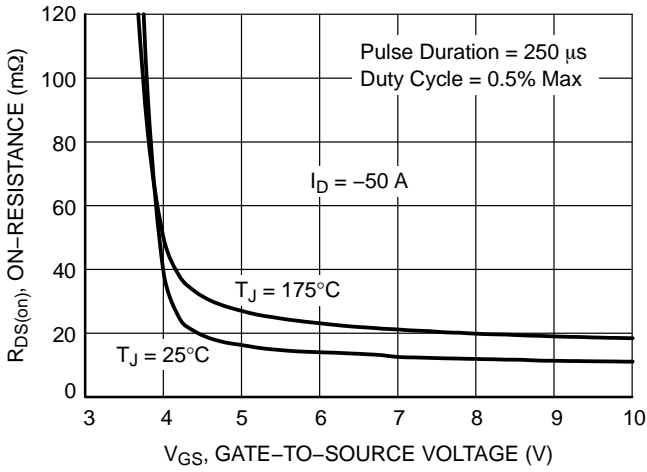


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

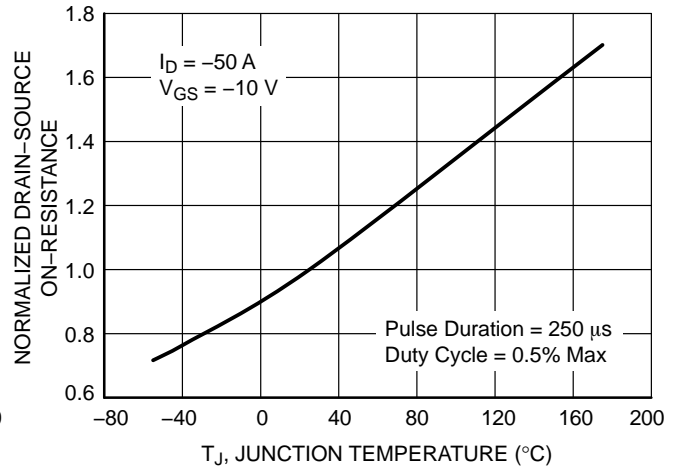


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

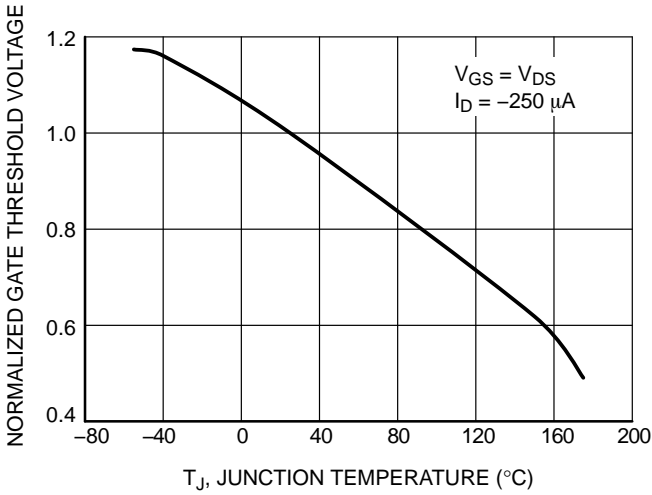


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

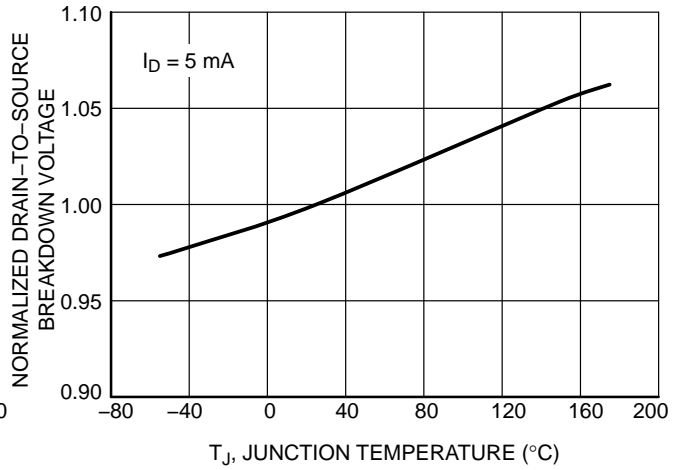


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

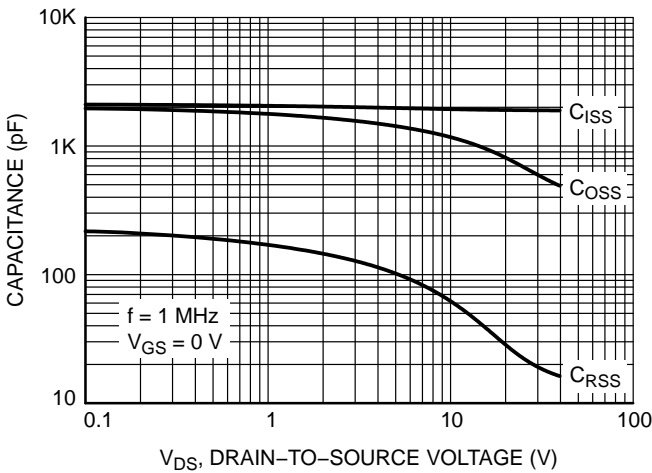


Figure 15. Capacitance vs. Drain-to-Source Voltage

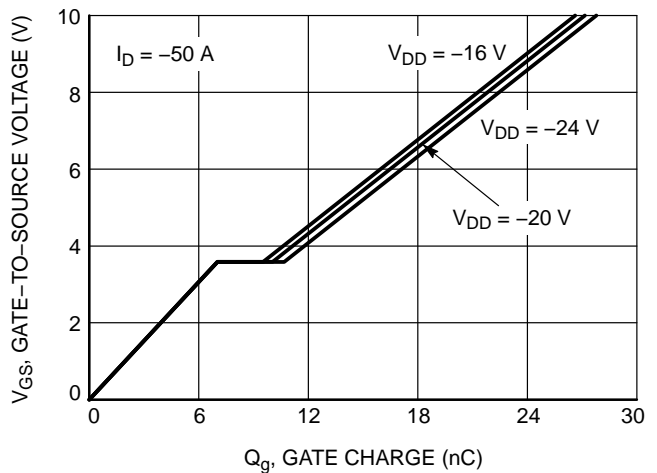
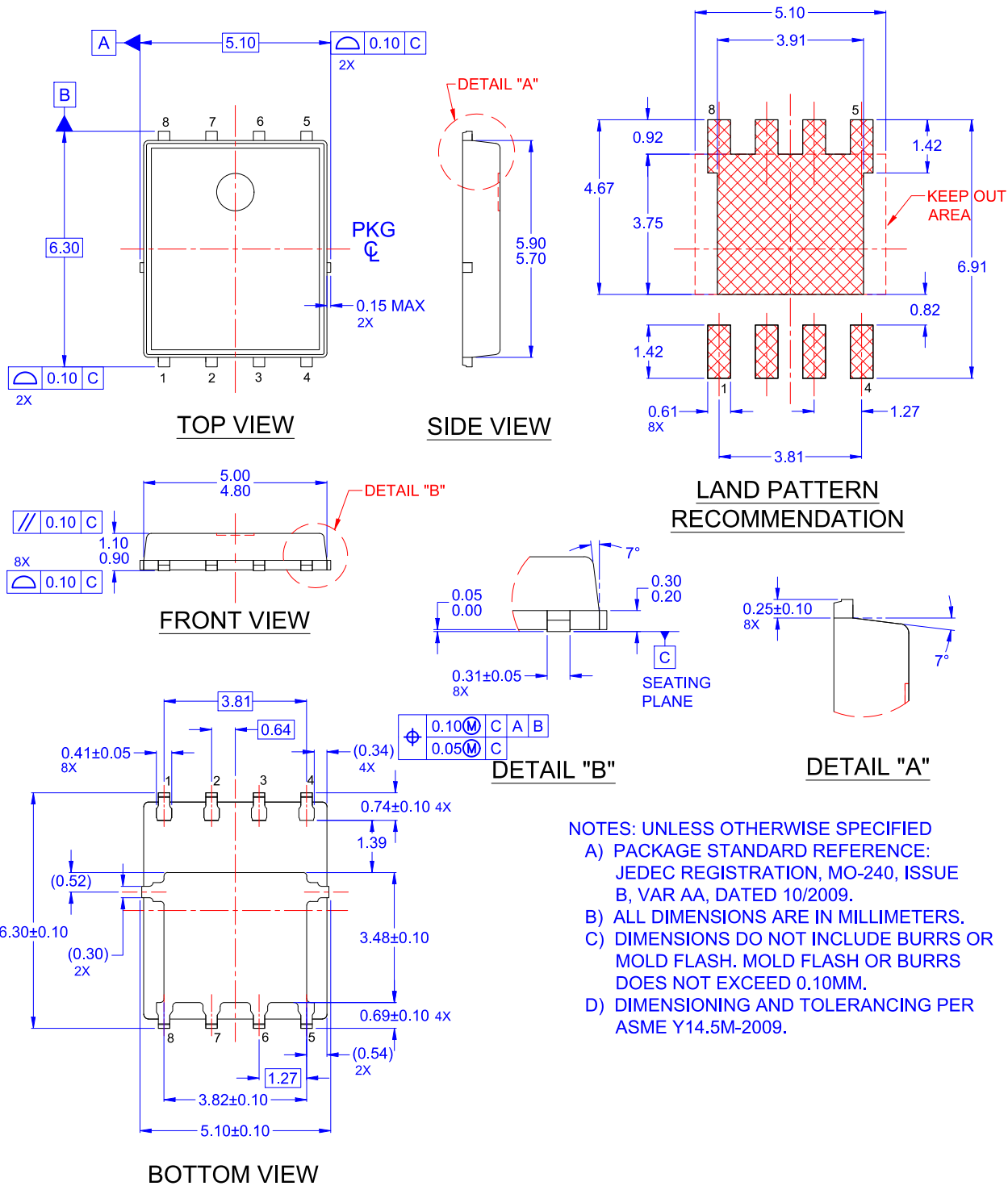


Figure 16. Gate Charge vs. Gate-to-Source Voltage

# FDWS9510L-F085


## PACKAGE DIMENSIONS

DFN8 5.1x6.3, 1.27P  
CASE 506DW  
ISSUE O



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, ISSUE B, VAR AA, DATED 10/2009.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

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